IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	**REDACTED PUBLIC VERSION**
Plaintiff,	)	
	)	C.A. No. 06-788 (JJF)
v.	)	
	)	~~**CONFIDENTIAL – SUBJECT TO PROTECTIVE ORDER**~~
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	~~**FILED UNDER SEAL**~~
	)	

APPENDIX TO OPENING BRIEF IN SUPPORT OF FREESCALE'S MOTION TO COMPEL PROMOS TO PROVIDE INFRINGEMENT CONTENTIONS AND LICENSING INFORMATION

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Dated: August 23, 2007
Redacted Filing Date: August 30, 2007

TABLE OF EXHIBITS

DESCRIPTION	EXHIBIT
ProMOS Technologies, Inc.'s Responses to Interrogatories Nos. 1-3 and 9, May 14, 2007, supplemental responses to 1-3 August 15, 2007	A
ProMOS's Claim Readings, May 14, 2007 • Attachment 1: 6,670,267 Fortin • Attachment 2: 5,488,709 Chan • Attachment 3: 5,732,241 Chan	B
ProMOS Technologies, Inc.'s Response to Interrogatory No. 18, July 25, 2007	C
ProMOS Technologies, Inc.'s Responses to Interrogatories Nos. 20 and 24, August 15, 2007	D
U.S. Patent 5,732,241 Chan (excerpts)	E
U.S. Patent 5,488,709 Chan (excerpts)	F
U.S. Patent 6,670,267 Fortin	G
Amendment, Fortin prosecution history, July 30, 2007 (pg. 9)	H
August 14, 2007 letter Michalik to Jensen	I
August 17, 2007 letter Jensen to Michalik	J
Freescale Semiconductor, Inc.'s Response to Interrogatory No. 19, August 16, 2007	K

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EXHIBIT A

CONFIDENTIAL EXHIBIT

EXHIBIT B

CONFIDENTIAL EXHIBIT

EXHIBIT C

IN THE UNITED STATES DISTRICT COURT
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PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	
	)	C.A. No. 06-788-JJF
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	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	

PLAINTIFF PROMOS TECHNOLOGIES, INC.'S OBJECTIONS AND RESPONSES TO DEFENDANT FREESCALE SEMICONDUCTOR, INC.'S SECOND SET OF INTERROGATORIES (No. 18)

Pursuant to Rules 26 and 36 of the Federal Rules of Civil Procedure, Plaintiff ProMOS Technologies, Inc. ("ProMOS") hereby submits the following objections and responses to Defendant Freescale Semiconductor, Inc.'s Second Set of Interrogatories (the "Requests").

GENERAL STATEMENT AND OBJECTIONS

ProMOS hereby incorporates by reference its General Statement and Objections from its Objections and Responses to Defendant Freescale Semiconductor, Inc.'s First Set of Interrogatories as though fully set forth herein.

RESPONSES AND SPECIFIC OBJECTIONS TO REQUESTS

ProMOS also expressly incorporates by reference its General Statement and Objections from its Objections and Responses to Defendant Freescale Semiconductor, Inc.'s First Set for Interrogatories in response to each of the following Requests and, to the extent they are not raised in any particular response, ProMOS does not waive those objections. In addition to the objections asserted therein, ProMOS responds as follows:

INTERROGATORY NO. 18:

State whether ProMOS contends that a fabrication method that includes the step of forming the claimed titanium nitride layer by chemical vapor deposition can infringe any claim of the '267 patent and, if so, identify which claims can be infringed by such method, and, for each such claim, state whether such method infringes that claim literally or under the doctrine of equivalents, provide all facts support such contention, and identify each person with knowledge of such facts.

RESPONSE TO INTERROGATORY NO. 18:

ProMOS objects to this request on the ground that it is premature and vague and ambiguous because the claims of the '267 patent have not yet been construed by the Court and Freescale has not defined the term "chemical vapor deposition." ProMOS also objects to this interrogatory on the ground that it is premature because it seeks expert opinion. ProMOS will disclose expert opinions at the time and in the manner contemplated by the Scheduling Order entered in this case.

Subject to and without waiving the foregoing general and specific objections, ProMOS states that the term "chemical vapor deposition" has not been defined by Freescale or clearly defined in the relevant art, nor is the line between chemical vapor deposition and physical vapor deposition well settled. Indeed, more recent developments in the art have blurred that line. Thus, a process that Freescale or others might characterize as "chemical vapor deposition" could in fact properly be understood to be or to include physical vapor deposition. Accordingly, absent a construction by the Court of the term "physical vapor deposition," or some other resolution of the extent of overlap and distinction between physical vapor deposition and chemical vapor deposition, it is not possible to know with certainty in the abstract whether a fabrication method that includes the step of forming the claimed titanium nitride layer by the latter may infringe one or more claims of the '267 patent literally or under the doctrine of equivalents.

ASHBY & GEDDES

/s/ *Lauren E. Maguire*

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Dated: July 25, 2007
182591.1

茂德科技股份有限公司
ProMOS TECHNOLOGIES, INC.

VERIFICATION TO PLAINTIFF PROMOS TECHNOLOGIES, INC.'S RESPONSES TO PLAINTIFF FREESCALE SEMICONDUCTOR, INC.'S <u>SECOND SET OF INTERROGATORIES (No. 18)</u>

I, Ming-Hsing Yang, declare under penalty of perjury that the following statements are true:

1. I am the Senior Manager at ProMOS Technologies, Inc. ("ProMOS") and am duly authorized to sign this verification on behalf of ProMOS.

2. I have read ProMOS's Responses to Freescale's Second Set of Interrogatories (No. 18), and am aware of its contents.

3. To the best of my knowledge, information, and belief founded upon reasonable inquiry, the factual contentions contained in these responses are true and correct and have evidentiary support or are likely to have evidentiary support after a reasonable opportunity for further investigation or discovery.

I declare under penalty of perjury under the laws of the United States of America that the forgoing is true and correct.

Executed on July 25, 2007

楊明興

Ming-Hsing Yang

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EXHIBIT D

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. 06-788-JJF
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant,	)	

PLAINTIFF PROMOS TECHNOLOGIES, INC.'S OBJECTIONS
AND RESPONSES TO FREESCALE'S THIRD SET OF INTERROGATORIES

Pursuant to Rules 26 and 33 of the Federal Rules of Civil Procedure, Rule 26.1 of the Local Rules of Civil Practice and Procedure of the United States District Court for the District of Delaware (hereinafter referred to as "Local Rules"), and the orders of this Court, plaintiff ProMOS Technologies, Inc. ("'ProMOS") hereby submits the following objections and responses to Freescale's Third Set of Interrogatories (the "Interrogatories").

GENERAL STATEMENT AND OBJECTIONS

ProMOS hereby incorporates by reference its General Statement and Objections from its Objections and Responses to Defendant Freescale Semiconductor, Inc.'s First Set of Interrogatories as though fully set forth herein.

RESPONSES AND SPECIFIC OBJECTIONS TO REQUESTS

ProMOS also expressly incorporates by reference its General Statement and Objections from its Objections and Responses to Defendant Freescale Semiconductor, Inc.'s First Set of Interrogatories in response to each of the following Interrogatories and, to the extent they are not raised in any particular response, ProMOS does not waive those objections. In addition to the objections asserted therein, ProMOS responds as follows:

ProMOS and Freescale representatives who attended the licensing negotiations with ProMOS have relevant knowledge regarding the information requested in this interrogatory. Documents related to Freescale's knowledge of the patents-in-suit include the ProMOS meeting minutes, ProMOS notice letters, and ProMOS powerpoint presentations that were previously produced to Freescale in this action.

INTERROGATORY NO. 20:

For each asserted claim of the '267 patent, state where with respect to the claimed opening (i.e., in the field, on the sidewalls of the opening, at the bottom of the opening, or otherwise) and when with respect to the steps in the claimed processes (i.e., immediately following deposition of the layer at issue, following the completion of the entire process, or otherwise) ProMOS contends layers of titanium and titanium nitride are to be measured, and identify the persons most knowledgeable about, and each document or thing supporting or otherwise relating to, such contention.

RESPONSE TO INTERROGATORY NO. 20:

ProMOS objects to this interrogatory to the extent that it seeks information that is protected from disclosure by the attorney client privilege and/or the work product doctrine. ProMOS also objects to this interrogatory on the ground that it is premature to the extent that it purports to seek disclosure of expert opinions. ProMOS will disclose its expert opinions at the time and in the manner required by the Federal Rules, the Local Rules and the Scheduling Order entered by the Court. ProMOS further objects to this interrogatory on the ground that it is premature in the absence of a claim construction ruling by the Court. Moreover, to the extent this is a "contention" interrogatory, ProMOS objects on the ground that it is untimely under the Scheduling Order because it was served after 6 p.m. EST on July 16 in violation of the parties' agreement regarding service procedures for this case.

Subject to and without waiving the foregoing general and specific objections, ProMOS responds that this interrogatory seeks ProMOS's contention on a claim construction issue. As

stated in response to Interrogatory No. 24 (which more directly seeks ProMOS's claim construction positions on all of the patents in suit), ProMOS would be willing to meet and confer with Freescale to establish a schedule pursuant to which the parties would simultaneously exchange proposed terms for construction, and then at a later date, proposed constructions for those terms, in advance of the date the parties' opening claim construction briefs are due.

INTERROGATORY NO. 21:

With respect to each Asserted Claim of the Patents-in-Suit, describe with specificity all grounds for ProMOS's contention that each such claim is not invalid, including without limitation a specific identification of each claim element which ProMOS contends is not present in each prior art reference identified by Freescale in this case and a specific, limitation-by-limitation rebuttal to the invalidity contentions set forth by Freescale in this case; identify the persons most knowledgeable about the facts supporting such grounds; and identify all documents supporting or otherwise relating to such facts.

RESPONSE TO INTERROGATORY NO. 21:

ProMOS objects to this interrogatory on the ground that it purports to alter the burden of proof that rests squarely on Freescale to demonstrate by clear and convincing evidence that one or more of the asserted claims of the patents-in-suit are invalid. ProMOS also objects to this interrogatory to the extent that it assumes – incorrectly – that Freescale has served "invalidity contentions." Freescale has responded to ProMOS's request for invalidity contentions merely by identifying a number of allegedly invalidating prior art references, without making any attempt to provide a limitation-by-limitation comparison of the prior art to the claims of the patents-in-suit. ProMOS further objects to this interrogatory on the ground that it is premature to the extent that it purports to seek disclosure of expert opinions. ProMOS will disclose its expert opinions at the time and in the manner required by the Federal Rules, the Local Rules and the Scheduling Order entered by the Court. Finally, ProMOS objects to this interrogatory to the extent that it seeks information that is protected from disclosure by the attorney client privilege and/or the

INTERROGATORY NO. 24:

For each claim of the Patents-in-Suit, provide in detail ProMOS's contentions of claim construction, state ProMOS's proposed construction of each word, term, or phrase of the claim and identify any of such constructions that is a special or uncommon meaning, state in detail the basis for ProMOS's construction, state each fact supporting or relating to ProMOS's construction, identify each reference or portion of the specification (including column and line or figure and label) or prosecution history that supports, describes, or explains ProMOS's construction and explain how, identify any extrinsic evidence that supports the construction, identify each person with knowledge relating to ProMOS's construction, and identify each document that reflects, or refers or relates to, ProMOS's construction.

RESPONSE TO INTERROGATORY NO. 24:

ProMOS objects to this interrogatory on the ground that it is premature. ProMOS is not required to disclose its claim construction positions until the date set forth in the Court’s Scheduling Order by which ProMOS must file its opening claim construction brief. ProMOS also objects to this interrogatory on the ground that it seeks information that is protected from disclosure by the attorney client privilege and/or the work product doctrine. ProMOS further objects to this interrogatory on the ground that it is premature to the extent that it purports to seek disclosure of expert opinions. ProMOS will disclose its expert opinions at the time and in the manner required by the Federal Rules, the Local Rules and the Scheduling Order entered by the Court. In addition, ProMOS objects to this interrogatory on the ground that it is overly broad and unduly burdensome and represents an untimely contention interrogatory. Moreover, to the extent this is a “contention” interrogatory, ProMOS objects on the ground that it is untimely under the Scheduling Order because it was served after 6 p.m. EST on July 16 in violation of the parties’ agreement regarding service procedures for this case.

Subject to and without waiving the foregoing general and specific objections, ProMOS states that it would be willing to meet and confer with Freescale to establish a schedule pursuant to which the parties would simultaneously exchange proposed terms for construction, and then at

a later date, proposed constructions for those terms, in advance of the date the parties' opening claim construction briefs are due.

<u>INTERROGATORY NO. 25</u>:

Identify and describe all opinions of counsel, validity or unenforceability searches, investigations or studies, and prior art made known to ProMOS relating to any or all of the Patents-in-Suit.

<u>RESPONSE TO INTERROGATORY NO. 25: -- OUTSIDE COUNSEL'S EYES ONLY</u>

ProMOS objects to this interrogatory on the ground that it seeks information that is protected from disclosure by the attorney client privilege and/or the work product doctrine. ProMOS also objects to this interrogatory on the ground that it is premature to the extent that it purports to seek disclosure of expert opinions. ProMOS will disclose its expert opinions at the time and in the manner required by the Federal Rules, the Local Rules and the Scheduling Order entered by the Court. ProMOS further objects to this interrogatory to the extent that it seeks information that is already known to Freescale. In addition, ProMOS objects to this interrogatory to the extent that it purports to require ProMOS to disclose information that is not within its possession, custody or control.

Subject to and without waiving the foregoing general and specific objections, ProMOS responds as follows: Freescale contends, in its answer to the complaint filed by ProMOS and in response to an interrogatory served by ProMOS, that certain prior art references invalidate the patents-in-suit. ProMOS will not repeat those contentions here as they are well known to Freescale. In addition, as previously described in ProMOS's response to Interrogatory No. 10, ProMOS has engaged in licensing discussions with Toshiba with respect to two of the patents-in-suit. During those discussions, Toshiba has alleged that United States Patent No. 4,208,716 invalidates the claims of the '241 patent.

EXHIBIT E

US005732241A

United States Patent [19]

Chan

[11] **Patent Number: 5,732,241**

[45] **Date of Patent: Mar. 24, 1998**

[54] **RANDOM ACCESS CACHE MEMORY CONTROLLER AND SYSTEM**

[75] Inventor: **Alfred K. Chan**, Milpitas, Calif.

[73] Assignee: **Mos Electronics, Corp.**, Sunnyvale, Calif.

[21] Appl. No.: **170,642**

[22] Filed: **Dec. 20, 1993**

Related U.S. Application Data

[63] Continuation of Ser. No. 678,914, Apr. 1, 1991, abandoned, which is a continuation-in-part of Ser. No. 546,071, Jun. 27, 1990, abandoned.

[51] **Int. Cl.**[6] **G06F 13/00**

[52] **U.S. Cl.** **395/458**

[58] **Field of Search** 395/427, 458

[56] **References Cited**

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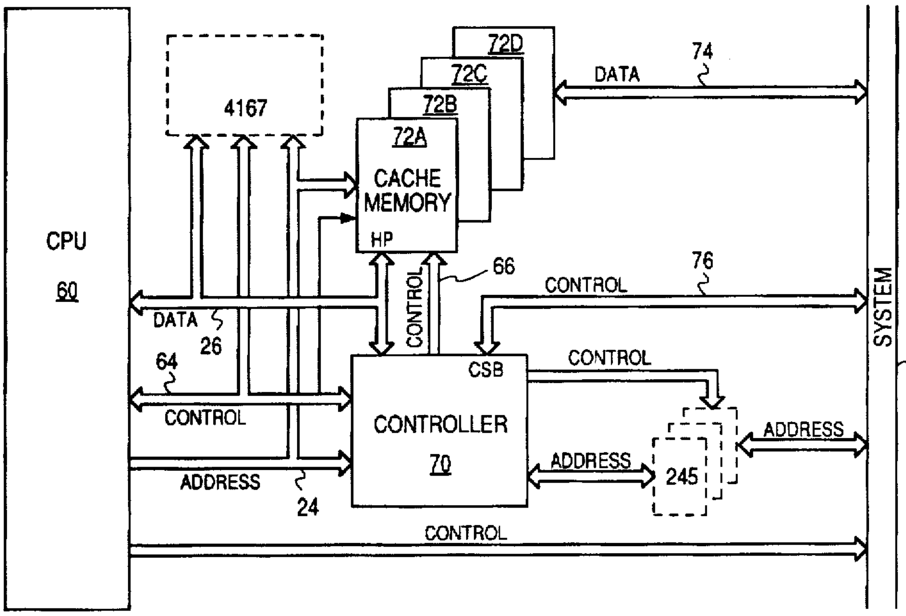
Intel Corporation, "i486 Microprocessor Hardware Manual", 1990, pp. 6–1 to 6–39.

Primary Examiner—David L. Robertson
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP

[57] **ABSTRACT**

A memory cache apparatus compatible with a wide variety of bus transfer types including non-burst and burst transfers. In burst mode, a "demand word first" wrapped around quad fetch order is supported. The cache memory system decouples the main memory subsystem from the host data bus so as to accommodate parallel cache-hit and system memory transfer operations for increased system speed and to hide system memory write-back cycles from the microprocessor. Differences in the speed of the local and system buses are accommodated, and an easy migration path from non-burst mode microprocessor based systems to burst mode microprocessor based systems is provided. Various memory organizations are accommodated including direct-mapped or one-way set associative, two-way set associative, and four-way set associative.

26 Claims, 70 Drawing Sheets



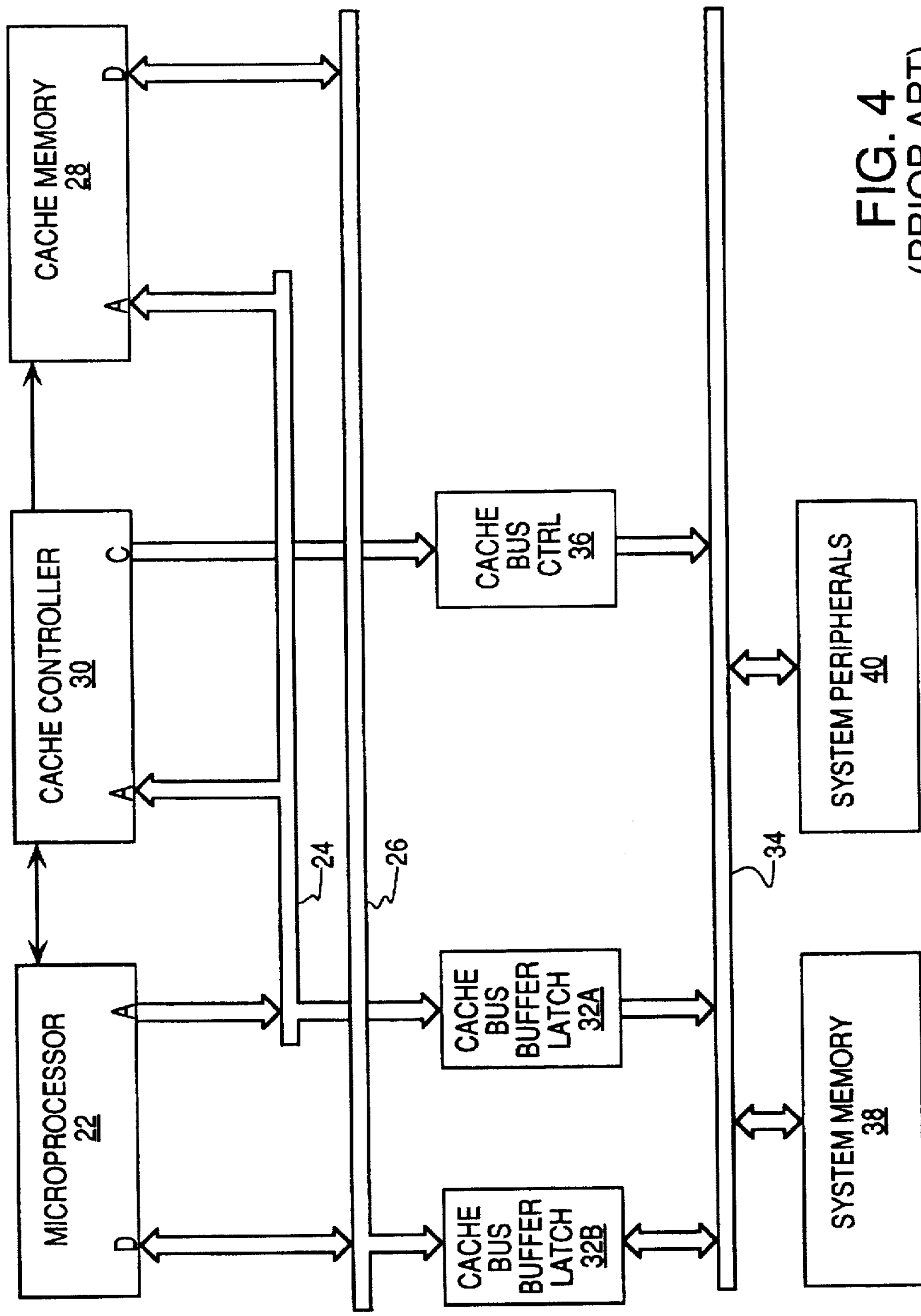


FIG. 4
(PRIOR ART)

cache, including support for non-cacheable accesses and multiple replacement cycles for lines longer than 16 bytes.

The cache memory **72** also supports quadword data fetch and, though not common in 386 systems, burst operation with main memory. If the cache and system memory controllers support burst operation, cache memory **72** will also support burst reads and writes to system memory **38**. In an 80386 system which is designed for future upgrade to an 80486, the main memory subsystem may use Intel's strongly suggested 64-bit, bank interleaved main memory organization. This memory organization is accessed using the non-sequential burst order used by the 486. Cache memory **72** directly supports that burst order to and from main memory, as well as the sequential burst order used with the smaller, less expensive, and standardized 32-bit sequential memory organization.

If the system memory uses the design-intensive 64-bit, bank interleaved architecture recommended by Intel instead of the standard, 32-bit sequential architecture, then the system port **112** uses the 486 burst sequence to system memory **38** instead of sequential order. Burst RAM cache memory **72** supports both sequential and 486 burst ordering. In either case, the fetch data from main memory is brought in "demand word first" such that the first doubleword passes directly to the 386 through each corresponding bypass path **119** of cache memory **72**. The 386 can then resume execution while the remainder of the burst data is brought in and stored in the RAM array **100**.

Numerous modifications and variations will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is to be understood that the above detailed description of the preferred embodiment is intended to be merely illustrative of the spirit and scope of the invention and should not be taken in a limiting sense. The scope of the claimed invention is better defined with reference to the following claims.

I claim:

1. A computer system comprising:

a host processor having a host address bus and a host data bus;

a system memory having storage locations addressable by said host processor, a system address bus and a system data bus;

a dual port cache memory having a system port connected to said system data bus and a host port connected to said host data bus, said dual port cache memory comprising cache storage locations dynamically associable with said storage locations of said system memory and a plurality of registers coupling said cache storage locations to said host port and said system port, wherein a data path between said host data bus and said system data bus is operably decoupled by buffering and selective provision of data to and from said cache storage locations by said plurality of registers so as to allow concurrent transfer of data to and from said dual port cache memory; and

a cache controller connected to said dual port cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said dual port cache memory and said cache controller are connected in parallel between said host processor and said system memory.

2. The computer system as recited in claim **1** wherein said cache controller is connected to said dual port cache memory for providing a first address on said host address bus concurrently with providing a second address on said system address bus, said first address corresponding to a different one of said storage locations of said system memory than said second address.

3. The computer system as recited in claim **1** wherein data on said host data bus is asynchronous to data on said system data bus.

4. The computer system as recited in claim **1** wherein said cache controller comprises:

a first control sequencer or controlling addressing and data signals on said host address bus and on said host data bus; and

a second control sequencer for controlling addressing and data signals on said system address bus and on said system data bus.

5. The computer system as recited in claim **1** further comprising means for disabling said dual port cache memory during a local bus access cycle.

6. The computer system as recited in claim **1** further comprising a peripheral device coupled to said system memory.

7. The computer system as recited in claim **6** wherein said peripheral device provides data to said system data bus, and wherein a hit address memory location within said dual port cache memory is loaded with said data from said peripheral device if the hit address of said dual port cache memory corresponds with an address of said data from said peripheral device.

8. The computer system as recited in claim **1** wherein said host processor operates at a first frequency, and wherein said system memory operates at a second frequency that is different from said first frequency.

9. A computer system according to claim **1** wherein said dual port cache memory comprises a plurality of burst random access memories.

10. A method for operating a memory cache apparatus, said memory cache apparatus including addressable storage, a host port, a system port, a host input register connected to said host port, a system input register connected to said system port, and a system output register connected to said system port, said method comprising the steps of:

receiving an address from a host;

comparing said received address to a plurality of addresses corresponding to cache data stored in said addressable storage;

placing a line of said cache data from a location in said addressable storage into said system output register;

placing data from said host into said host input register;

wherein if said received address does not match one of said plurality of addresses corresponding to said cache data:

placing said host data into said location in said addressable storage from said host input register;

receiving system data corresponding to said received address from said system port into said system input register; and

subsequent to said step of placing said host data into said addressable storage, and without overwriting said host data, placing said system data corresponding to said received address from said system input register into said location in said addressable storage.

11. The computer system as recited in claim **4** wherein said host microprocessor operates at a first frequency, and wherein said system memory operates at a second frequency that is different from said first frequency.

12. The method for operating a cache memory apparatus as recited in claim **10**, wherein data from a plurality of data

locations of said addressable storage are placed in said system output register during a single clock cycle.

13. The method for operating a cache memory apparatus as recited in claim **10**, further comprising the step of coupling said host port to said system port when a read miss cycle occurs.

14. The method for operating a memory cache apparatus as recited in claim **10**, wherein said step of placing data from said host into said host input register occurs in a first clock cycle, and wherein said step of placing said host data into said location in said addressable storage occurs on a second clock cycle, said second clock cycle immediately following said first clock cycle.

15. A computer system comprising:

a host processor having a host address bus and a host data bus for providing a host address and host data;

a system memory for storing system data, said system memory having a system data bus for providing system data;

a dual port cache memory for storing said host data and system data, said dual port cache memory including:

addressable memory storage;

a host input register coupled to said addressable memory storage and to said host data bus for providing data from said host data bus to said addressable memory storage; and

a system input register coupled to said addressable memory storage and to said system data bus for receiving a line of said cache data from said data bus and providing said line of cache data to said addressable memory storage; and

a controller connected to said dual port cache memory and said host address bus, said controller containing a plurality of addresses corresponding to said cache data for receiving said host address from said host address bus and comparing said host address to said plurality of addresses, wherein when a match results from said comparing:

host data from said host input register is placed into said addressable memory storage at a location of said line of cache data; and

system data from said system input register is placed into said location of said line of cache data after said host data is placed into said addressable memory storage, wherein said host data is not overwritten.

16. A computer system comprising:

a host microprocessor having a host address bus and a host data bus;

a system memory having a system address bus and a system data bus;

a dual port cache memory including:

addressable storage,

a host port coupled to the host data bus,

a system port coupled to the system data bus,

a first input register for selectively writing input data to said addressable storage, said first input register being coupled between said host port and said addressable storage,

a first output register for selectively furnishing output data to said system port, said first output register being coupled between said addressable storage and said system port, said input data being provided to said addressable storage from said first input register at the same time that said output data is provided by said first output register to said system port,

a second input register for providing second input data to said addressable storage, said second input register being coupled between said addressable storage and said system port, and

a second output register coupled between said addressable storage and said host port for providing second output data from said addressable storage to said host port, said second input data being provided to said addressable storage from said second input register at the same time that said second output data is provided by said second output register to said system port; and

a cache controller connected to said dual port cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said cache memory and said cache controller are connected in parallel between said host processor and said system memory,

said cache controller being connected to said dual port cache memory for providing a first address on said host address bus concurrently with providing a second address on said system address bus, said first address corresponding to a different memory location than said second address.

17. The computer system as recited in claim **16** wherein data on said host data bus is asynchronous to data on said system data bus.

18. The computer system as recited in claim **16** wherein said cache controller comprises:

a first control sequencer for controlling addressing and data signals on said host address bus and on said host data bus; and

a second control sequencer for controlling addressing and data signals on said system address bus and on said system data bus.

19. The computer system as recited in claim **16** further comprising means for disabling said dual port cache memory during a local bus access cycle.

20. The computer system as recited in claim **16** further comprising a peripheral device coupled to said system memory.

21. The computer system as recited in claim **20** wherein said peripheral device provides data to said system data bus, and wherein a hit address memory location within said dual port cache memory is loaded with said data from said peripheral device if the hit address of said dual port cache memory corresponds with an address of said data from said peripheral device.

22. The computer system as recited in claim **16** wherein said host microprocessor operates at a first frequency, and wherein said system memory operates at a second frequency that is different from said first frequency.

23. An apparatus as recited in claim **16** further comprising a bypass path coupled between said host port and said system port for directly allowing passage of data between said host port and said system port.

24. An apparatus as recited in claim **16**, wherein said first input register is a memory write register, said second input register is an update register, said first output register is a write back register, and said second output register is a read hold register.

25. The cache memory apparatus as recited in claim **16** wherein said second input register can store a plurality of words of data.

26. The cache memory apparatus as recited in claim **25** further comprising means for masking writing of selected words of data into said random access memory.

* * * * *

EXHIBIT F

US005488709A

United States Patent [19]

Chan

[11] **Patent Number: 5,488,709**

[45] **Date of Patent: Jan. 30, 1996**

[54] **CACHE INCLUDING DECOUPLING REGISTER CIRCUITS**

[75] Inventor: **Alfred K. Chan**, Milpitas, Calif.

[73] Assignee: **MOS Electronics, Corp.**, Sunnyvale, Calif.

[21] Appl. No.: **678,912**

[22] Filed: **Apr. 1, 1991**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 546,071, Jun. 27, 1990, abandoned.

[51] **Int. Cl.**[6] **G06F 13/00**; G06F 13/28

[52] **U.S. Cl.** **395/445**; 395/458; 395/470; 395/476; 395/250

[58] **Field of Search** 395/425, 250, 395/470, 476, 458, 445

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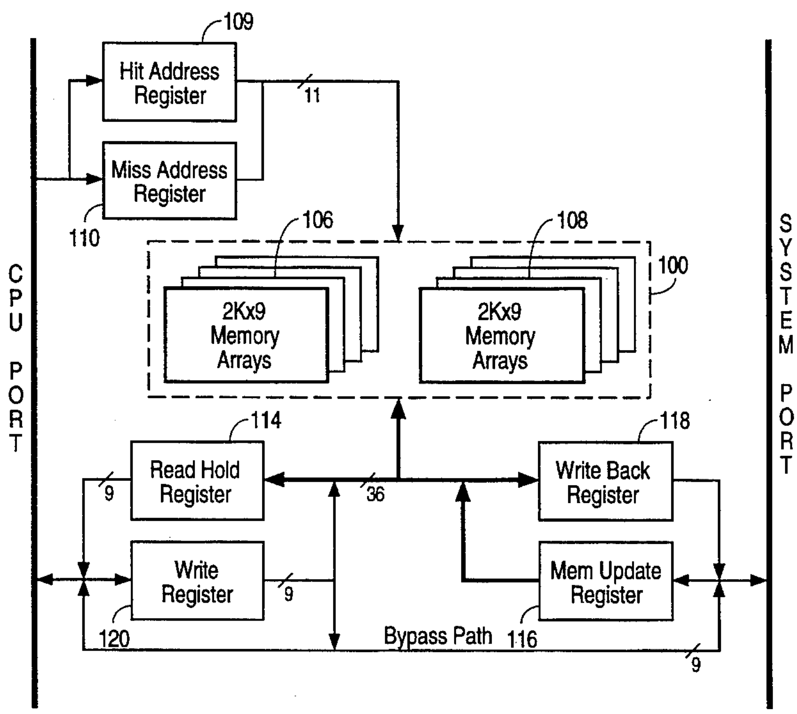
Primary Examiner—Glenn Gossage
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel

[57] **ABSTRACT**

A memory cache apparatus compatible with a wide variety of bus transfer types including non-burst and burst transfers. The memory cache apparatus includes a random access memory, a host port, and a system port. The memory cache apparatus further includes an input register connected to the host port for selectively writing data to the random access memory and an output register connected to the system port for receiving data from the random access memory and selectively furnishing the data to the host port or the system port. In one embodiment, the input register is a memory write register, and the output register includes a read hold register and a write back register. A cache memory system decouples a main memory subsystem from a host data bus so as to accommodate parallel cache-hit and system memory transfer operations for increased system speed and to hide system memory write-back cycles from a microprocessor. Differences in the speed of the local and system buses are accommodated, and an easy migration path from non-burst mode microprocessor based systems to burst mode microprocessor based systems is provided. Various memory organizations are accommodated including direct-mapped or one-way set associative, two-way set associative, and four-way set associative.

26 Claims, 68 Drawing Sheets



fetched first, eliminating what would be a large replacement time penalty.

It is also noted that port **113** interfaces with the Intel **386** or **486** processor in a manner similar to conventional SRAMs. If data parity is not checked as in most **386** systems, HP<8> and SP<8> can be left disconnected.

By decoupling the host and system data buses **112** and **113**, processor cache accesses and system memory accesses can proceed simultaneously. Decoupling on a write-back cache allows write misses to be handled with zero wait states since read and write cache hits can proceed in parallel with the write miss data fetching. Moreover, when combined with the procedure implemented by each burst RAM memory chip for saving write-back data during read or write misses, the dual-port architecture allows write-back line replacement cycles to be completely hidden from the processor.

When used in sets of four, the burst RAM memory chips allow internal data transfers of four doublewords (128 bits) on reads or writes, achieving a true 128-bit quadword transfer in only one clock. When doing memory burst operations, the internal structure of the burst RAM memory chip behaves similar to a static column RAM in that the input buffer and word line delays occur only on the first access to the first subarray. Subsequent accesses in the burst are supplied by successive subarrays which are pre-addressed. This structure allows full speed burst accesses without the use of 10 nsec SRAMs.

The architecture of burst RAM cache memory **72** eliminates the historical disadvantage of write-back caches: having to do a replace cycle before doing the data fetch. With burst RAM cache memory **72**, the replace data is saved within a set of latches of the burst RAM memory chips (memory write back registers **118**A–**118**D) as soon as a miss is detected and thus allows the fetch to begin immediately. Only after the fetch is complete does a replacement cycle begin, and during that time, the host processor **60** can resume accessing the cache RAM array **100** through the host port **113**. As an example, in a system with a two wait state memory and non-burst fetches, the use of burst RAM cache memory **72** allows the **386** to be operating at full speed after a read miss in just 5 clocks. Using standard SRAMs, the same system would take 48 clocks (32 clocks for two lines on a tag miss plus 16 clocks for the new data).

Decoupled buses also avoids the necessity to redesign the system memory subsystem every time the processor module is upgraded. In fact, the processor data bus and the system data bus can run at different speeds. Since the processor will work out of its cache subsystem more than 95% of the time, the system memory need not be redesigned to run at the same speed as the processor. This is especially true if the system uses a burst memory controller so that the cache memories can support burst operation to and from system memory. The main memory system might then operate at a reasonably easy to design speed of 20 MHz, while the processor module (processor, cache controller, and cache memories) operates at 25, 33, or even 40 MHz. Upgrading the processor from an **80386** to an **80486** would involve only minor design changes to main memory.

Also noted above, both of the 9-bit (eight bits plus parity) data ports **112** and **113** of each burst RAM memory chip support "demand word first" wrapped around quadword operations as well as scalar reads and writes. The system port **112** supports burst operations to and from system memory **38** if the system memory controller also supports burst.

The dual-port architecture of the burst RAM cache memory chip permits processor and main memory accesses

to occur in parallel, while hiding write-back cycles from the processor, contributing to a substantial performance increase over alternative implementations. The burst RAM cache memory chip fully supports an **80386** using a write-back cache, including support for non-cacheable accesses and multiple replacement cycles for lines longer than 16 bytes.

The cache memory **72** also supports quadword data fetch and, though not common in 386 systems, burst operation with main memory. If the cache and system memory controllers support burst operation, cache memory **72** will also support burst reads and writes to system memory **38**. In an **80386** system which is designed for future upgrade to an **80486**, the main memory subsystem may use Intel's strongly suggested 64-bit, bank interleaved main memory organization. This memory organization is accessed using the non-sequential burst order used by the **486**. Cache memory **72** directly supports that burst order to and from main memory, as well as the sequential burst order used with the smaller, less expensive, and standardized 32-bit sequential memory organization.

If the system memory uses the design-intensive 64-bit, bank interleaved architecture recommended by Intel instead of the standard, 32-bit sequential architecture, then the system port **112** uses the **486** burst sequence to system memory **38** instead of sequential order. Burst RAM cache memory **72** supports both sequential and **486** burst ordering. In either case, the fetch data from main memory is brought in "demand word first" such that the first doubleword passes directly to the **386** through each corresponding bypass path **119** of cache memory **72**. The **386** can then resume execution while the remainder of the burst data is brought in and stored in the RAM array **100**.

Numerous modifications and variations will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is to be understood that the above detailed description of the preferred embodiment is intended to be merely illustrative of the spirit and scope of the invention and should not be taken in a limiting sense. The scope of the claimed invention is better defined with reference to the following claims.

I claim:

1. A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a memory write register for buffering first data received from said host port and selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port, said memory write register being coupled between said host port and said random access memory and between said host port and said system port; and

a write back register for holding second data received from said random access memory and selectively providing the second data to said system port, said write back register being coupled between said random access memory and said system port;

wherein the buffering and selective providing of the first data to said random access memory and the holding and selective providing of the second data to said system port allows memory accesses at said host port to be decoupled from memory accesses at said system port.

2. The cache memory apparatus as recited in claim **1** further comprising a read hold register coupled between said random access memory and said host port for buffering and providing burst read data from said random access memory to said host port.

3. The cache memory apparatus as recited in claim **1** further comprising a bypass path coupled between said host port and said system port for directly allowing passage of data between said host port and said system port.

4. The cache memory apparatus as recited in claim **1** wherein said random access memory includes storage for a plurality of parity bits.

5. The cache memory apparatus as recited in claim **1** wherein said random access memory is organized in a plurality of lines wherein each of said lines comprises a plurality of word storage locations, and wherein each of said word storage locations is selectively writable.

6. The cache memory apparatus as recited in claim **1** wherein said random access memory is written using a read-modify-write operation.

7. The cache memory apparatus as recited in claim **1** wherein said random access memory is single ported.

8. The cache memory apparatus as recited in claim **7** wherein said random access memory is accessed with a wider bandwidth than said host port and said system port.

9. An apparatus as in claim **1**, further comprising a memory update register for holding fetched data and providing the fetched data to said random access memory, said memory update register being coupled between said random access memory and said system port, wherein the holding and selective providing of the second data and the holding of the fetched data allows write back and fetch operations at said system port to be decoupled from said random access memory.

10. The cache memory apparatus as recited in claim **9** further comprising means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the second data held in said write back register for write back to said system port, said identifying means being selective for the ones of the fetched data to be provided from said memory update register to said random access memory.

11. The cache memory apparatus as recited in claim **9** wherein said memory update register can store a plurality of words of the fetched data.

12. The cache memory apparatus as recited in claim **11** further comprising means for masking the providing of selected ones of said words of the fetched data to said random access memory.

13. A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a memory write register coupled to said random access memory, to said host port, and to said system port for buffering and selectively providing input data received from said host port to one of said random access memory, said system port, and said random access memory and said system port; and

a write back register coupled to said system port and to said random access memory for holding output data received from said random access memory and selectively providing said output data to said system port;

wherein the input data is provided to said random access memory from said memory write register at the same time that the output data is provided by said write back register to said system port, the buffering and selective providing of the input data to said random access memory and the holding and selective providing of the output data to said system port allowing memory accesses at said host port to be decoupled from memory accesses at said system port.

14. The cache memory apparatus as recited in claim **13** further comprising:

a miss address register coupled to said host port and to said random access memory for storing a cache miss address signal corresponding to a word of the output data to be received from said random access memory into said write back register; and

a hit address register coupled to said host port and to said random access memory for storing a cache hit address signal selective for a word stored in said random access memory.

15. The cache memory apparatus as recited in claim **14** further comprising a counter coupled to said miss address register.

16. The cache memory apparatus as recited in claim **15** wherein said counter increments from an address associated with a first line of data to an address associated with a subsequent line of data.

17. A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a memory write register for buffering and selectively writing first input data to said random access memory, said memory write register being coupled between said host port and said random access memory;

a write back register for holding and selectively furnishing first output data to said system port, said write back register being coupled between said random access memory and said system port, the first input data being provided to said random access memory from said memory write register at the same time that the first output data is provided by said write back register to said system port, the selective writing of the first input data to said random access memory and the selective furnishing of the first output data to said system port allowing memory accesses at said host port to be decoupled from memory accesses at said system port;

a memory update register for holding and selectively providing second input data to said random access memory, said memory update register being coupled between said random access memory and said system port, wherein the holding and selective furnishing of the first output data and the holding and selective providing of the second input data allows write back and memory update operations at said system port to be decoupled from said random access memory; and,

a read hold register coupled between said random access memory and said host port for providing second output data from said random access memory to said host port, the second input data being provided to said random access memory from said memory update register at the same time that the second output data is provided by said read hold register to said host port.

18. An apparatus as recited in claim **17** further comprising a bypass path coupled between said host port and said system port for directly allowing passage of data between said host port and said system port.

19. The cache memory apparatus as recited in claim **17** wherein said memory update register can store a plurality of words of the second input data.

20. An apparatus as recited in claim **17**, wherein the first input data comprises memory write data, the second input data comprises system fetch data, the first output data comprises system write back data, and the second output comprises burst read data.

21. The cache memory apparatus as recited in claim **20** further comprising means for masking writing of selected words of the system fetch data into said random access memory.

22. A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a bypass path coupled between said host port and said system port for directly passing data between said host port and said system port;

a memory write register for buffering and selectively providing memory write data to one of said random access memory, said system port via said bypass path, and said random access memory and said system port via said bypass path, said memory write register being coupled to said bypass path and between said host port and said random access memory;

a write back register for holding and selectively furnishing write back data to said system port, said write back register being coupled between said random access memory and said system port, said write back register allowing the write back data to be furnished to said system port at the same time that said memory write register provides the memory write data to said random access memory;

a memory update register for holding and selectively providing system fetch data to said random access memory, said memory update register being coupled between said random access memory and said system port, wherein the holding and selective furnishing of the write back data and the holding and selectively providing of the system fetch data allows write back and memory update operations at said system port to be decoupled from said random access memory; and

a read hold register coupled between said random access memory and said host port for buffering and providing burst read data from said random access memory to said host port, said read hold register allowing the burst read data to be provided to said host port at the same time that said memory update register provides the system fetch data to said random access memory.

23. The cache memory apparatus as recited in claim **22** wherein said memory update register can store a plurality of words of the system fetch data.

24. The cache memory apparatus as recited in claim **22** further comprising means for masking writing of selected words of the system fetch data into said random access memory.

25. The cache memory apparatus as recited in claim **22** further comprising:

a miss address register coupled to said host port and to said random access memory for storing a cache miss address signal, the cache miss address signal being selective for words of the fetch data to be received into said memory update register and corresponding to words of the write back data to be held in said write back register and replaced in said random access memory by the words of fetch data; and

a hit address register coupled to said host port and to said random access memory for storing a cache hit address signal selective for a word stored in said random access memory.

26. The cache memory apparatus as recited in claim **22** further comprising means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port, said identifying means being selective for the ones of the fetched data to be provided from said memory update register to said random access memory.

* * * * *

EXHIBIT G

US006670267B2

(12) **United States Patent**
Fortin

(10) **Patent No.: US 6,670,267 B2**
(45) **Date of Patent: Dec. 30, 2003**

(54) **FORMATION OF TUNGSTEIN-BASED INTERCONNECT USING THIN PHYSICALLY VAPOR DEPOSITED TITANIUM NITRIDE LAYER**

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(73) Assignee: **Mosel Vitelic Inc.**, Hsin Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/881,607**

(22) Filed: **Jun. 13, 2001**

(65) **Prior Publication Data**

US 2003/0001265 A1 Jan. 2, 2003

(51) **Int. Cl.**[7] **H01L 21/4763**; H01L 29/12

(52) **U.S. Cl.** **438/629**; 438/637; 438/667; 438/700; 257/915

(58) **Field of Search** 257/758, 752, 257/753, 774, 775, 915; 438/118, 222, 622, 690–693, 687, 758, 316, 632–634, 720, 784, 629, 637, 643, 644, 667, 750, 700

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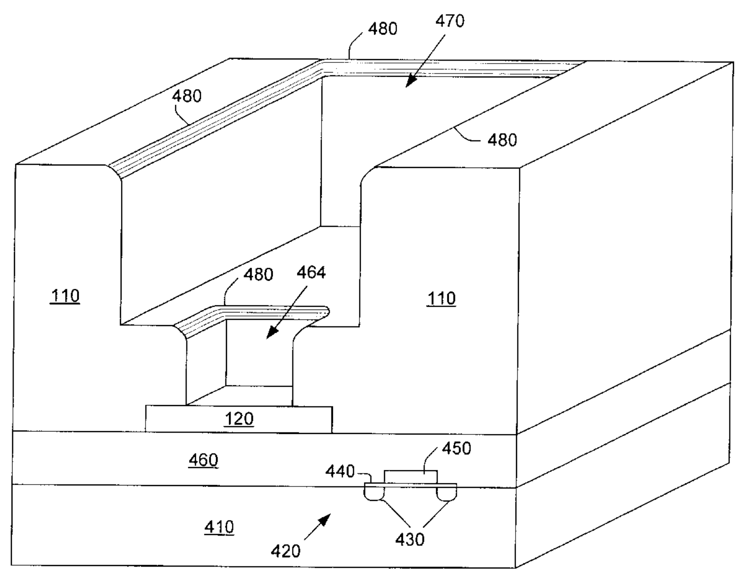
Primary Examiner—David Nelms
Assistant Examiner—Long Tran
(74) *Attorney, Agent, or Firm*—Ronald J. Meetin

(57) **ABSTRACT**

A tungsten-based interconnect is created by first providing a structure with an opening (**464**/**470**) in a structure and then rounding the top edge of the opening. A titanium nitride layer (**150**) is physically vapor deposited to a thickness less than 30 nm, typically less than 25 nm, over the structure and into the opening. Prior to depositing the titanium nitride layer, a titanium layer (**140**) may be deposited over the structure and into the opening such that the later-formed titanium nitride layer contacts the titanium layer. In either case, the titanium nitride layer is heated, typically to at least 600° C., while being exposed to nitrogen and/or a nitrogen compound. A tungsten layer (**160**) is subsequently chemically vapor deposited on the titanium nitride layer and into the opening.

54 Claims, 4 Drawing Sheets



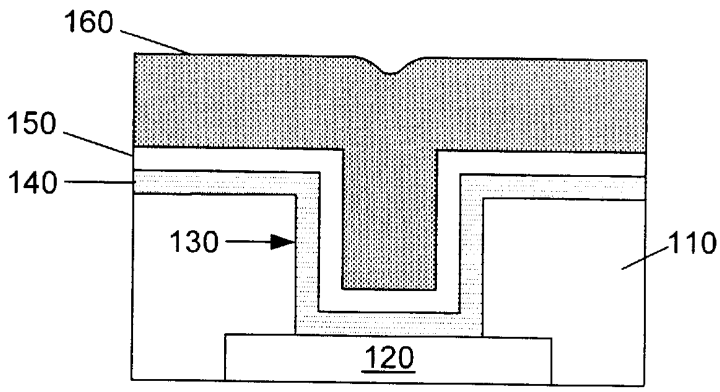


FIG. 1 PRIOR ART

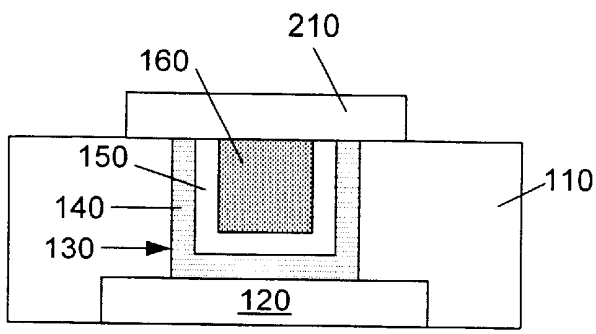


FIG. 2 PRIOR ART

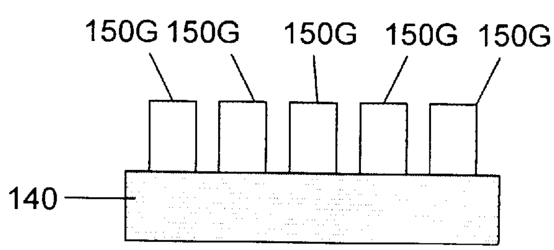


FIG. 3 PRIOR ART

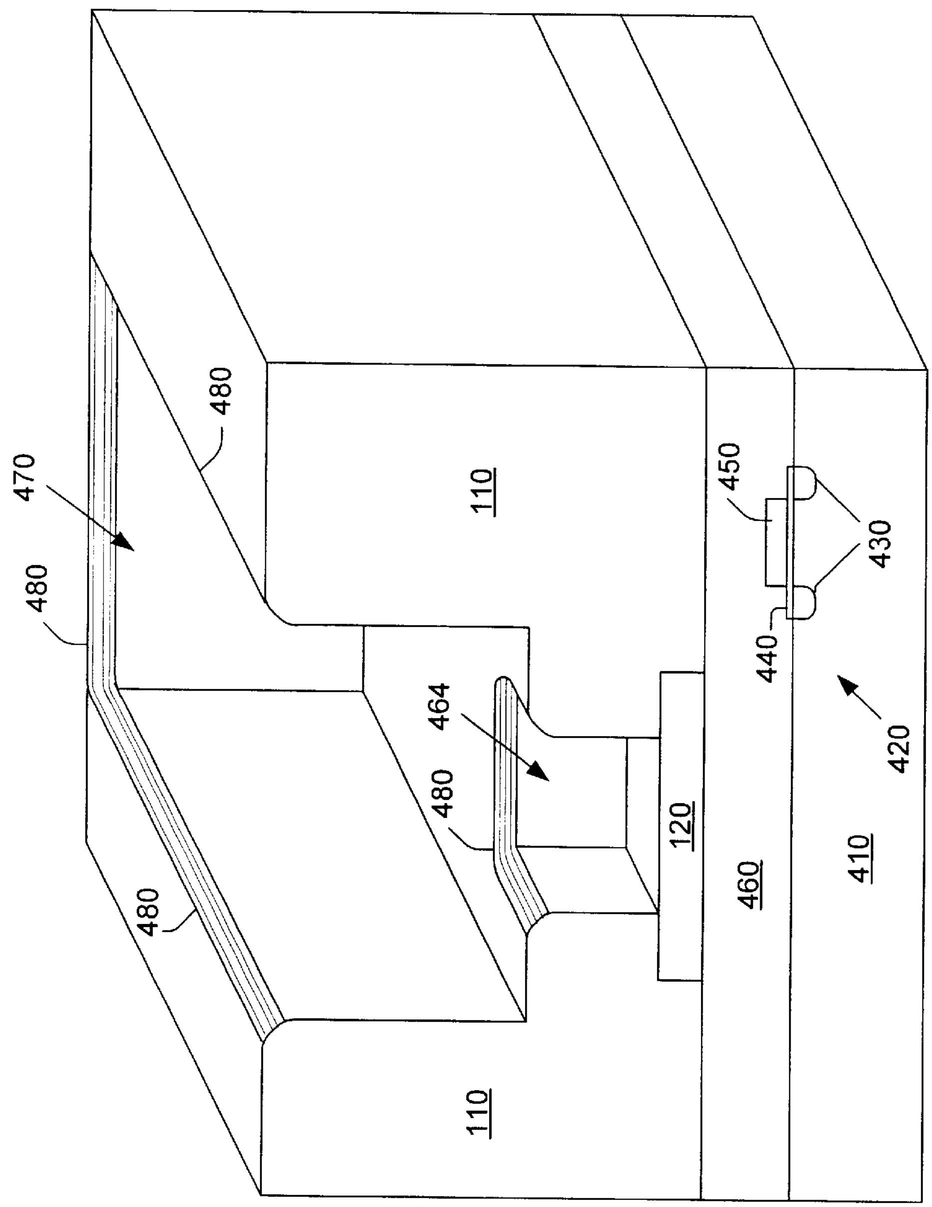


FIG. 4

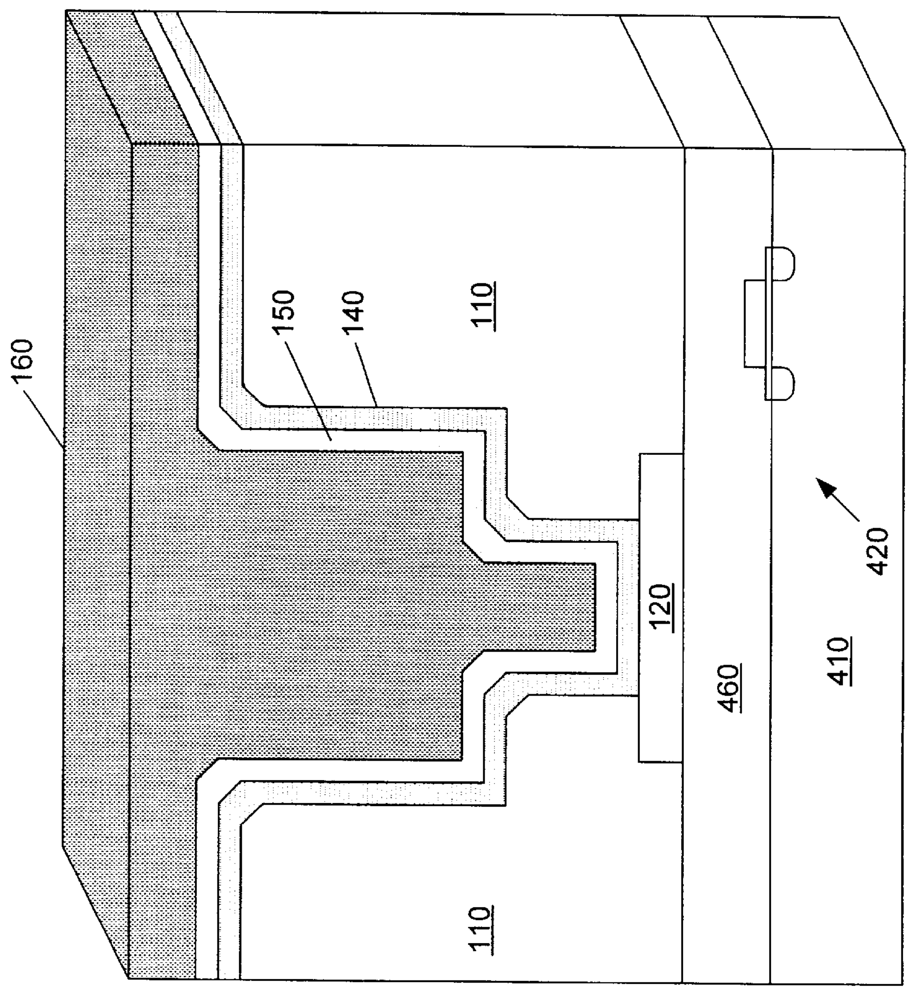


FIG. 5

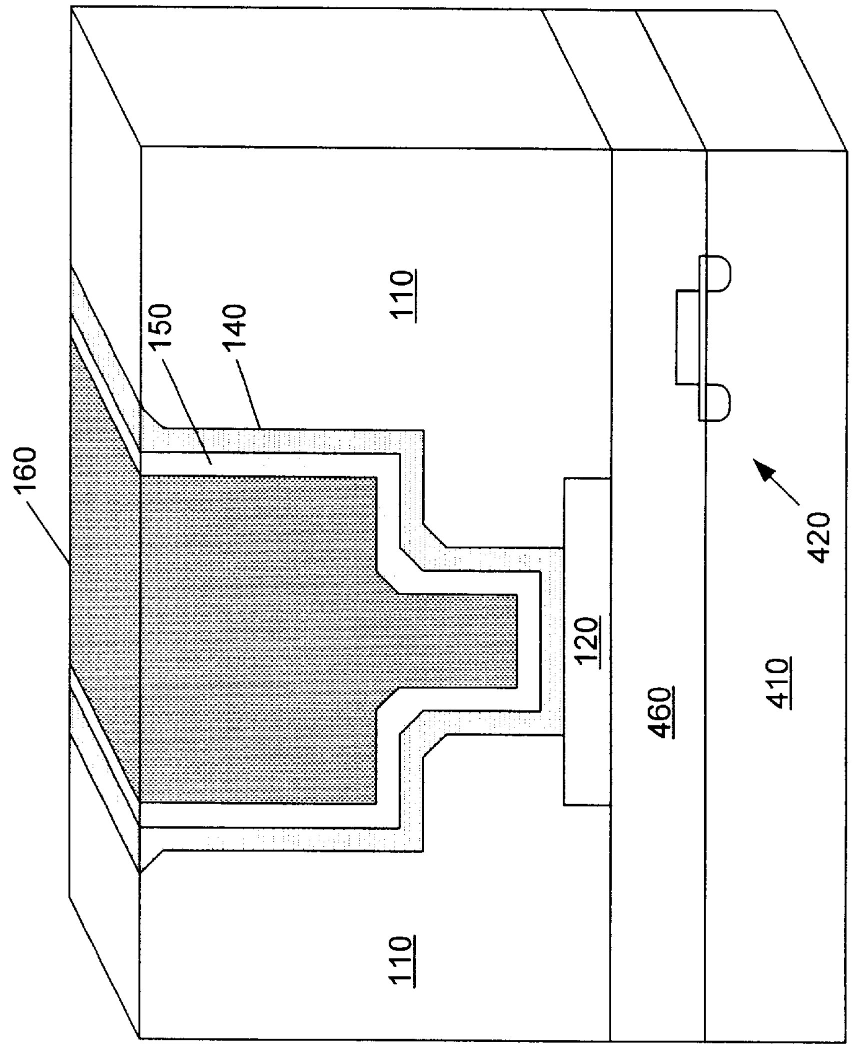


FIG. 6

FORMATION OF TUNGSTEIN-BASED INTERCONNECT USING THIN PHYSICALLY VAPOR DEPOSITED TITANIUM NITRIDE LAYER

BACKGROUND

The present invention relates to physical vapor deposition of titanium nitride.

Titanium nitride has been used as a barrier and adhesion layer in fabrication of tungsten plugs in semiconductor integrated circuits. Tungsten plugs interconnect different conductive layers separated by a dielectric. Frequently used dielectrics are silicon dioxide and silicon nitride. Tungsten does not adhere well to silicon dioxide and silicon nitride, so titanium nitride has been used to promote adhesion. In addition, titanium nitride serves as a barrier layer preventing a chemical reaction between WF_6 (a compound from which the tungsten is deposited in a chemical vapor deposition process) and other materials present during tungsten deposition. See "Handbook of Semiconductor Manufacturing Technology" (2000), edited by Y. Nichi et al., pages 344–345.

FIGS. **1**, **2** illustrate a typical fabrication process. A dielectric layer **110** is deposited over a layer **120** which can be a metal or silicon layer. A via **130** is etched in the dielectric. A thin titanium layer **140** is deposited over dielectric **110** and into the via **130** to improve contact resistance (the titanium dissolves the native oxide on layer **120**). Then titanium nitride layer **150** is deposited. Then tungsten **160** is deposited by chemical vapor deposition (CVD) from tungsten hexafluoride (WF_6). Tungsten **160** fills the via. Layers **160**, **150**, **140** are removed from the top surface of dielectric **110** (by chemical mechanical polishing or some other process). See FIG. **2**. The via remains filled, so the top surface of the structure is planar. Then a metal layer **210** is deposited. The layers **160**, **150**, **140** in via **130** provide an electrical contact between the layers **210** and **120**.

Titanium nitride **150** can be deposited by a number of techniques, including sputtering and chemical vapor deposition (CVD). Sputtering is less complex and costly (see "Handbook of Semiconductor Manufacturing Technology", cited above, page 411), but the titanium nitride layers deposited by sputtering have a more pronounced columnar grain structure. FIG. **3** illustrates columnar monocrystalline grains 150 G in titanium nitride layer **150**. During deposition of tungsten **160**, the WF_6 molecules can diffuse between the TiN grains and react with titanium **140**. This reaction produces titanium fluoride TiF_3. TiF_3 expands and causes failure of the TiN layer. The cracked TiN leads to a higher exposure of TiF_3 to WF_6, which in turn leads to the formation of volatile TiF_4. TiF_4 causes voids in the W film which are known as "volcanoes". To avoid the volcanoes, the sputtered titanium nitride layers have been made as thick as 40 nm, and at any rate no thinner than 30 nm. In addition, the sputtered titanium nitride layers have been annealed in nitrogen atmosphere to increase the size of the TiN grains.

SUMMARY

The inventor has determined that under some conditions thinner annealed layers of sputtered titanium nitride unexpectedly provide better protection against the volcanoes than thicker layers. In some embodiments, fewer volcanoes have been observed with a TiN layer thickness of 20 nm than with 30 nm. In fact, no volcanoes have been observed in some structures formed with the 20 nm TiN layers. Why the thinner TiN layers provide better protection is not clear. Without limiting the invention to any particular theory, it is suggested that perhaps one reason is a lower stress in the thinner annealed layers and a higher density of the TiN grains.

The invention is applicable to physical vapor deposition techniques other than sputtering. Additional features and embodiments of the invention are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**–**3** are cross sectional views of prior art semiconductor structures in the process of fabrication.

FIGS. **4**–**6** are cross sectional and perspective views of semiconductor structures in the process of fabrication according to one embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **4** is a cross sectional and perspective view of a dual damascene semiconductor structure in the process of fabrication according to one embodiment of the present invention. Layer **120** is polysilicon formed by chemical vapor deposition (CVD) over a monocrystalline silicon wafer **410**. Before fabrication of layer **120**, the wafer **410** may have been processed to form devices such as MOS transistor **420**. The transistor's source/drain regions **430** were formed in substrate **410**, gate insulation **440** was formed over the substrate, and gate **450** was formed over the gate insulation. Other devices, including non-MOS devices, could be formed using known techniques. Layer **120** can also be part of substrate **410** (this embodiment is not shown in FIG. **4**).

In the embodiment of FIG. **4**, dielectric **460** was deposited over the wafer. Then layer **120** was formed as described above, and was patterned by a plasma etch. An exemplary thickness of layer **120** is 150 nm.

Dielectric layer **110** was deposited over the layer **120**. In some embodiments, dielectric **110** was a combination of two silicon dioxide layers. The first layer was PSG (phosphosilicate glass) deposited by chemical vapor deposition (CVD). The second layer was silicon dioxide deposited by CVD from TEOS. The combined thickness of the two layers was approximately 900 nm.

Then a photoresist layer (not shown) was deposited and patterned photolithographically to define a via **464**. In some embodiments, the mask opening defining the via was round in top view, with a diameter of 0.18 μm. The via was formed in layer **110** with a plasma etch.

The photoresist was removed, and another layer of photoresist (not shown) was deposited and patterned photolithographically to define a trench **470** in dielectric **110** for a tungsten interconnect. The length of the trench **470** was normally at least 2 μm. In some embodiments, the trench length was approximately 1 mm. The trench width was then 0.22 μm. The trench was etched with a timed etch to a depth of approximately 250 nm. Via **464** was fully exposed at the bottom of the trench.

Then the top surface of the structure was exposed to RF plasma in argon atmosphere for 10 seconds. The argon flow was 5 sccm (standard cubic centimeters per minute). The RF power was 315 W. This operation removed native oxide from layer **120**. Also, this operation smoothened (rounded) top edges **480** of trench **470** and via **464**, i.e., the respective perimetrical top edges formed by the perimeters of trench **470** and via **464** along the surfaces into which they respectively extend. The rounded perimetrical top edges are desir-

able to reduce stress in titanium nitride **150** (FIG. **5**) at these edges so as to reduce the risk of volcano formation. The RF plasma operation was performed in a system of type ENDURA available from Applied Materials of Santa Clara, Calif.

Then titanium layer **140** (FIG. **5**) was sputter deposited from a titanium target. The sputtering was performed at a temperature of 200° C. in argon atmosphere. The base pressure (the pressure before the argon flow was turned on) was 5×10^{-7} torr. The DC power was 4000 W, the RF power was 2500 W. The wafer AC bias was 150 W. The titanium deposition was performed in a system of type ENDURA, in an ionized metal plasma (IMP) chamber of type Vectra, available from Applied Materials.

The thickness of Ti layer **140** was varied. In one embodiment, the thickness was less than 36 nm, preferably less than 15 nm, more preferably less than 12 nm, typically 10 nm. In another embodiment, the thickness was 36 nm.

Then titanium nitride **150** was deposited by reactive sputtering from a titanium target in a nitrogen atmosphere. The base pressure (the pressure before the nitrogen flow was turned on) was 5×10^{-7} torr. The nitrogen flow was 28 sccm (standard cubic centimeters per minute), the DC power was 4000 W, the RF power was 2500 W, the wafer bias was 150 W. The deposition temperature was 200° C. The deposition was performed in a system of type ENDURA, in an IMP chamber of type Vectra, available from Applied Materials.

In one embodiment, the thickness of TiN layer **150** was less than 30 nm, preferably less than 25 nm, more preferably less than 22 nm, typically 20 nm. The thickness of the TiN layer **150** was 30 nm in another embodiment.

Then the structure was heated to a temperature between 600° C. and 700° C. for 20 to 40 seconds, typically 20 to 30 seconds, in a nitrogen atmosphere. (This operation is referred to herein as Rapid Thermal Anneal, or RTA.) The base pressure was 100–120 torr, the nitrogen flow was **8** slm (standard liters per minute). The temperature was 620° C. in one embodiment, 670° C. in another embodiment. The anneal was performed in a system of type HEATPULSE 8800 available from AG Associates, Inc., of San Jose, Calif. The anneal is believed to have increased the lateral size of TiN grains 150G (FIG. **3**).

Then tungsten layer **160** was deposited by CVD in two stages. At the first stage, the chemical reaction was:

$$2WF_6+3SiH_4\rightarrow 2W+3SiF_4+6H_2$$

This stage lasted 10 seconds. Then the silane (SiH_4) flow was turned off, and the hydrogen flow was turned on for the second stage. The chemical reaction was:

$$WF_6(\text{vapor})+3H_2\ (\text{vapor})\rightarrow W(\text{solid})+6HF(\text{vapor}).$$

See S. Wolf, "Silicon Processing for the VLSI Era", vol. 2 (1990), page 246, incorporated herein by reference. Both stages were performed in a system of type CONCEPT 1 available from Novellus Systems of San Jose, Calif. The silane flow was 20 sccm. The hydrogen flow was 12–15 slm (standard liters per minute). The WF_6 flow was 350 sccm. The pressure was 40 torr. The temperature was 400° C.

Then the layers **160**, **150**, **140** were polished off the top of dielectric **110** by CMP. The resulting structure is shown in FIG. **6**. Prior to CMP, the structure was examined for volcanoes using an optical microscope and SEM and STEM microscopes. The results are given in Table 1 below. The second column of Table 1 indicates the temperature of the Rapid Thermal Anneal, described above, performed after the

deposition of TiN **150** before the deposition of tungsten **160**. In Embodiment No. 1, the anneal was omitted.

TABLE 1

Embodiment No.	RTA of TiN	Ti/TiN thickness: 10 nm/20 nm Volcanoes observed?	Ti/TiN thickness: 36 nm/30 nm Volcanoes observed?
1.	None	Yes	Yes
2.	620° C.	No	Yes, but fewer than in Embodiment No. 1
3.	670° C.	No	No

These results show, unexpectedly, that the use of thinner Ti and TiN layers in combination with the RTA can provide a better protection against the volcanoes than thicker layers without the RTA. The thinner layers can eliminate the volcanoes at the lower RTA temperature of 620° C. Lower RTA temperatures are desirable to reduce impurity diffusion during the RTA, to prevent melting or softening of materials having low melting temperatures (e.g. aluminum), and reduce wafer warping. In any event, the sputter deposited TiN layers, such as TiN layer **150**, have substantially a columnar grain structure.

The invention is not limited to the particular materials, dimensions, structures, or fabrication processes described above. The invention is not limited to a thickness or composition of any particular layer, or the number, shape and size of vias **464** or trenches **470**. The trench length, for example, is 2 μm in some embodiments, and other lengths are possible. The invention is not limited to the particular gas flow rates, temperatures, or any other fabrication parameters or equipment. Some embodiments use nitrogen sources other than pure nitrogen for the RTA or titanium nitride deposition. For example, ammonia (NH_3) or H_2/N_2 can be used. The invention is not limited to the Rapid Thermal Anneal or to any particular anneal temperature. Non-rapid anneals can be used. The anneal can be performed with plasma or with other heating techniques, known or to be invented. The invention is applicable to TiN sputtered from a TiN target. The invention is applicable to single damascene, dual damascene, and other structures, for example, to tungsten plugs formed in contact vias in non-damascene structures, and to tungsten features other than plugs. Titanium **140** is omitted in some embodiments. The invention is applicable to different tungsten CVD techniques, including tungsten deposition from WCl_6 rather than WF_6. The invention is not limited by particular materials chosen for the layers **120**, **110**, **460**. Some embodiments involve non-silicon semiconductor materials. The invention is not limited to any particular sputtering process, and further is applicable to TiN deposited by physical vapor deposition techniques other than sputtering. For example, pulsed laser deposition and other evaporation techniques can be used. See "Handbook of Semiconductor Manufacturing Technology" (2000), cited above, pages 395–413, incorporated herein by reference. Layer **120** (FIG. **4**) can be a metal layer, and can be part of the second, third, or higher metallization layers. The term "layer", as used herein, may refer to a combination of two or more other layers. The invention is defined by the appended claims.

I claim:

1. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 25 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

2. The method of claim **1** wherein the titanium nitride layer is formed by sputtering.

3. The method of claim **2** wherein the titanium nitride layer is less than 22 nm thick.

4. The method of claim **2** wherein the titanium nitride layer is about 20 nm thick.

5. The method of claim **1** further comprising, before forming the titanium nitride layer, forming a titanium layer over the structure such that the titanium layer extends at least into the opening in the structure, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

6. The method of claim **5** wherein the titanium layer is less than 36 nm thick.

7. The method of claim **5** wherein the titanium layer is about 10 nm thick.

8. The method of claim **1** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of at least 600° C.

9. The method of claim **1** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 670° C. for 20–40 seconds.

10. The method of claim **1** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 620° C. for 20–40 seconds.

11. The method of claim **1** wherein:

the structure comprises (a) a substrate, (b) a circuit element situated in or over the substrate, and (c) an insulating layer situated over the circuit element and the substrate, the opening in the structure comprising an opening in the insulating layer, the opening in the insulating layer comprising a trench at least 2 μm long;

the titanium nitride layer and the tungsten layer extend into the opening in the insulating layer; and

the tungsten layer electrically contacts the circuit element through material of the titanium nitride layer in the opening in the insulating layer.

12. The method of claim **11** wherein the substrate is a semiconductor substrate.

13. The method of claim **12** wherein the trench is at least 1 mm long.

14. The method of claim **13** further comprising, before forming the titanium nitride layer, depositing a titanium layer over the insulating layer such that the titanium layer extends at least into an opening in the insulating layer and such that the tungsten layer electrically contacts the circuit element through material of the titanium and titanium nitride layers in the opening in the insulating layer.

15. The method of claim **14** wherein the trench does not penetrate the insulating layer but a via at the bottom of the trench penetrates the insulating layer and exposes the circuit element, wherein the titanium layer physically contacts the circuit element at the bottom of the via.

16. The method of claim **13** wherein the circuit element is conductive.

17. The method of claim **13** wherein the circuit element comprises metal or semiconductor material.

18. The method of claim **13** wherein the opening in the structure includes a via at the bottom of the trench, the method further comprising rounding the via along its perimetrical top edge.

19. A structure formed by the method of claim **1**.

20. The structure of claim **19** wherein the titanium nitride layer has a substantially columnar grain structure.

21. A structure formed by the method of claim **2**.

22. The structure of claim **21** wherein the titanium nitride layer has a substantially columnar grain structure.

23. The method of claim **1** where the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

24. The method of claim **23** wherein the tungsten halide comprises tungsten hexafluoride.

25. A method for fabricating an integrated circuit, the method comprising:

forming a circuit element in or over a semiconductor substrate;

forming an insulating layer over the circuit element;

forming an opening through the insulating layer to expose the circuit element at the bottom of the opening, the opening having a perimetrical top edge that extends along an exterior surface of the insulating layer;

rounding the top edge of the opening;

forming a titanium layer over the insulating layer, the titanium layer overlaying side and bottom surfaces of the opening, the titanium layer being less than 15 nm thick;

forming a titanium nitride layer over the titanium layer, the titanium nitride layer being less than 25 nm thick, the titanium nitride layer being formed by sputtering;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and

forming a tungsten layer by chemical vapor deposition over the titanium nitride layer, the tungsten layer at least partially filling the opening and electrically contacting the circuit element through the titanium and titanium nitride layers.

26. The method of claim **25** wherein the opening comprises a trench at least 2 μm long.

27. The method of claim **25** wherein the opening comprises a trench at least 1 mm long.

28. The method of claim **25** wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a temperature of about 670° C. for 20–40 seconds.

29. The method of claim **25** wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a temperature of about 620° C. for 20–40 seconds.

30. The method of claim **25** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of at least 600° C.

31. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride

layer extends at least into the opening, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer to a temperature above 600° C. while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

32. The method of claim **31** wherein the titanium nitride layer is formed by sputtering.

33. The method of claim **31** further comprising, before forming the titanium nitride layer, forming a titanium layer over the structure such that the titanium layer extends at least into the opening in the structure, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

34. The method of claim **33** wherein the titanium layer is less than 36 nm thick.

35. The method of claim **31** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 670° C. for 20–40 seconds.

36. The method of claim **31** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 620° C. for 20–40 seconds.

37. The method of claim **31** wherein:

the structure comprises (a) a substrate, (b) a circuit element situated in or over the substrate, and (c) an insulating layer situated over the circuit element and the substrate, the opening in the structure comprising an opening in the insulating layer, the opening in the insulating layer comprising a trench at least 2 μm long;

the titanium nitride layer and the tungsten layer extend into the opening in the insulating layer; and

the tungsten layer electrically contacts the circuit element through material of the titanium nitride layer in the opening in the insulating layer.

38. The method of claim **37** wherein the substrate is a semiconductor substrate.

39. The method of claim **38** wherein the trench is at least 1 mm long.

40. The method of claim **39** further comprising, before forming the titanium nitride layer, depositing a titanium layer over the insulating layer such that the titanium layer extends at least into an opening in the insulating layer and such that the tungsten layer electrically contacts the circuit element through material of the titanium and titanium nitride layers in the opening in the insulating layer.

41. The method of claim **40** wherein the trench does not penetrate the insulating layer but a via at the bottom of the trench penetrates the insulating layer and exposes the circuit element, wherein the titanium layer physically contacts the circuit element at the bottom of the via.

42. The method of claim **39** wherein the opening in the structure includes a via at the bottom of the trench, the method further comprising rounding the via along its perimetrical top edge.

43. A structure formed by the method of claim **31**.

44. The structure of claim **43** wherein the titanium nitride layer has a substantially columnar grain structure.

45. The method of claim **31** where the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

46. The method of claim **45** wherein the tungsten halide comprises tungsten hexafluoride.

47. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

48. The method of claim **47** wherein the titanium nitride layer is formed by sputtering.

49. The method of claim **47** further comprising, before forming the titanium nitride layer, forming a titanium layer over the structure such that the titanium layer extends at least into the opening in the structure, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

50. The method of claim **47** wherein the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

51. The method of claim **50** wherein the tungsten halide comprises tungsten hexafluoride.

52. A fabrication method comprising:

forming a titanium nitride layer over a structure by physical vapor deposition such that the titanium nitride layer extends at least into an opening in the structure, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening, the chemical vapor deposition of the tungsten layer comprising reacting a tungsten halide with silane and subsequently with hydrogen.

53. The method of claim **52** wherein the tungsten halide comprises tungsten hexafluoride.

54. The method of claim **52** wherein the titanium nitride layer is formed by sputtering.

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EXHIBIT H

#7A
7/30/02
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE
JUL 17 2002
PATENT & TRADEMARK OFFICE

Applicant:	Fortin, Vincent		
Assignee:	Mosel Vitelic, Inc.		
Title:	Thin Titanium Nitride Layers Used In Conjunction With Tungsten		
Serial No.:	09/881,607	Filing Date:	June 13, 2001
Examiner:	Tran, Long K.	Group Art Unit:	2818
Docket No.:	M-11469 US		

San Jose, California
July 17, 2002

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Washington, D.C. 20231

AMENDMENT

Sir:

Responsive to the Office Action mailed 23 April 2002, please amend the above patent application as follows:

IN THE SPECIFICATION

Page 2, amend the paragraph beginning on line 11 to read

--The inventor has determined that under some conditions thinner annealed layers of sputtered titanium nitride unexpectedly provide better protection against the volcanoes than thicker layers. In some embodiments, fewer volcanoes have been observed with a TiN layer thickness of 20 nm than with 30 nm. In fact, no volcanoes have been observed in some structures formed with the 20 nm TiN layers. Why the thinner TiN layers provide better protection is not clear. Without limiting the invention to any particular theory, it is suggested that perhaps one reason is a lower stress in the thinner annealed layers and a higher density of the TiN grains.--

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substrate to a thickness of 5 - 100 nm and that titanium nitride layer 24 is formed on titanium nitride layer 22 likewise to a thickness of 5 - 100 nm. The composite thickness for titanium nitride layers 22 and 24 would thus appear to be 10 - 200 nm. However, Fiordalice discloses that layers 22 and 24 are formed by chemical vapor deposition ("CVD"), not physical vapor deposition ("PVD").

More particularly, Fiordalice states at col. 2, lines 56 - 61, that titanium nitride layer 22 is chemically vapor deposited. Slightly later at col. 2, lines 63 - 66, Fiordalice specifies that the deposition ambient, i.e., the vapor which acts as a source for the material deposited during Fiordalice's CVD, includes titanium tetrachloride, ammonia, nitrogen (diatomic), and argon.

Fiordalice does not appear to expressly state that titanium nitride layer 24 is chemical vapor deposited. However, Fiordalice states at col. 3, lines 43 - 51, that titanium nitride layer 24 is deposited *in situ* with titanium nitride layer 22 using a deposition ambient that includes titanium tetrachloride, ammonia, nitrogen, and argon. Since the deposition ambient utilized to form layer 24 is that same at that used to chemically vapor deposit layer 22, layer 24 is also formed by CVD. Hence, both of titanium nitride layers 22 and 24 are formed by CVD.

CVD is a deposition process in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface. In the preferred embodiment of Fiordalice, titanium nitride layers 22 and 24 are formed by chemical reaction in which the titanium tetrachloride undergoes chemical reaction to release titanium atoms which react chemically with nitrogen atoms provided from the ammonia and possibly the (diatomic) nitrogen.

PVD is a general term for a deposition process in which the material to be deposited is released from the source of the material largely by one or more physical mechanisms. Examples of PVD include sputtering, evaporation, pulsed laser deposition, and spraying.

In any event, CVD is not PVD or a type of PVD. Since Fiordalice discloses that titanium nitride layers 22 and 24 are formed by CVD, the material which extends from col. 2, line 21, through col. 4, line 17, of Fiordalice, and which includes the portion of Fiordalice

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EXHIBIT I

CONFIDENTIAL EXHIBIT

EXHIBIT J

CONFIDENTIAL EXHIBIT

EXHIBIT K

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC., Plaintiff, v. FREESCALE SEMICONDUCTOR, INC., Defendant.	)	C.A. No. 06-788 (JJF)

DEFENDANT FREESCALE'S RESPONSE TO PLAINTIFF PROMOS TECHNOLOGIES, INC.'S FOURTH SET OF INTERROGATORIES TO DEFENDANT FREESCALE SEMICONDUCTOR, INC. (NOS. 19-20)

Pursuant to Rules 26 and 33 of the Federal Rules of Civil Procedure, Defendant Freescale Semiconductor, Inc. ("Freescale") responds as follows to Plaintiff ProMOS Technologies, Inc.'s Fourth Set Of Interrogatories To Defendant Freescale Semiconductor, Inc. (Nos. 19-20), served by ProMOS Technologies, Inc. ("ProMOS").

GENERAL OBJECTIONS

Freescale hereby repeats and incorporates by reference its General Objections set forth in its Defendant Freescale's Response To Plaintiff ProMOS Technologies, Inc.'s First Set Of Interrogatories To Defendant Freescale Semiconductor, Inc. (Nos. 1-14).

SPECIFIC OBJECTIONS AND RESPONSES

INTERROGATORY NO. 19:

For each claim of the Patents-in-Suit, provide in detail Freescale's contentions of claim construction, state Freescale's proposed construction of each word, term, or phrase of the claim and identify any of such constructions that is a special or uncommon meaning, state in detail the basis for Freescale's construction, state each fact supporting or relating to Freescale's construction, identify each reference or portion of the specification (including column and line or figure and label) or prosecution history that supports, describes, or explains Freescale's construction and explain how, identify any extrinsic evidence that supports the construction, identify each person with knowledge relating to Freescale's construction, and identify each document that reflects, or refers or relates to, Freescale's construction.

RESPONSE:

In addition to its General Objections, Freescale objects to this interrogatory as premature because ProMOS has the burden of proof and yet has failed to provide any detail with regard to its infringement contentions.

Without waiving any, and subject to all, of its General and Specific Objections, Freescale responds that, having brought and maintained this action against Freescale alleging infringement of the three Patents-in-Suit, ProMOS has the burden to set forth reasonable contentions of claim scope and infringement. Yet ProMOS has not done so. Instead, it has persisted in this litigation without giving meaningful contentions. For example, ProMOS has refused to provide meaningful claim charts (or any claim charts for most claims) setting forth actual contentions regarding which Freescale products infringe which patent claims and explaining how the limitations of the claims are allegedly met. Without this fundamental information, it is impossible for Freescale to identify the claim terms it believes must be construed. ProMOS's failure to provide contentions is particularly egregious because ProMOS's position in this litigation conflicts squarely with statements made by the inventors to the United States Patent and Trademark Office limiting the scope of their patent claims and with other direct evidence that ProMOS's assertions of infringement are unfounded.

<u>THE CHAN PATENTS</u>

ProMOS for months persisted in pursuing the two Chan Patents-in-Suit broadly against Freescale's entire product line, seeking in depth discovery of essentially all documents and concerning essentially all of Freescale's products. To support that improper discovery, ProMOS described the Chan patents in exceedingly broad terms, characterizing them as the "cache memory patents" and as "involve[ing] cache memory," which ProMOS defined as "a

supplementary system that temporarily stores frequently used instructions and data for quicker processing by the central processor of the computer." (ProMOS's motion to compel, DI 29, pp. 1-2). Based on that overbroad scope, ProMOS sought discovery of all "Freescale Products," defined by ProMOS without limitation as including all "microcontrollers, microprocessors, processors, digital signal processors, controller cores, processor cores *or other components or goods that use, incorporate, work with or rely on cache memory*." (Ex. A to ProMOS's motion, p. 5) (emphasis added). In other words, ProMOS attempted to obtain discovery of all products of any kind that use cache memory in any way, in plain disregard of the actual, limited scope of the Chan patent claims.

Yet the Chan patents are very narrow in scope in view of the extensive prior art and the statements made and positions taken in the PTO in order to procure issuance of the patents over the prior art. As acknowledged in the Chan patents themselves, cache memory had been used in semiconductor technology for years before the Chan patents. Contrary to ProMOS's position, the Chan patents clearly cannot be construed to cover all uses of cache memories for many reasons, including the following:

First, the claims of Chan '709 are directed to a cache memory apparatus having a particular structure and functionality, and the claims of Chan '241 are directed to "computer systems" containing, among other things, the particular Chan cache claimed in the Chan '709 patent in combination with a cache controller configured in a special manner. Those limitations cannot be ignored.

Second, the specification makes clear the limited scope of the Chan patents. For example, Figure 4 of each patent specification identifies as "prior art" a computer system with a cache memory and cache controller, thus emphasizing that only very particular systems of cache

memories and controllers could possibly be within the scope of the Chan patents. As another example, the Chan specification acknowledges that the prior art Intel 486 microprocessor, the product for which the Chan embodying product was developed, was provided with an embedded cache memory.

Third, because cache memories were so well-known prior to the Chan patents, the inventor had a difficult time convincing the PTO to grant the two Chan patents. With the Chan '709 patent, which is directed to a cache memory apparatus with particular structure and functionality, the inventor amended the claims 4 times before the PTO would grant the patent. Acquiescing to the fact that most limitations of its cache apparatus claims were found in the prior art cited by the PTO, the inventor argued that the distinguishing feature of the claims was not just any cache memory, but instead "a cache memory which includes a memory write register for buffering data received from a host port and selectively providing that data to a RAM, to a system port, or to both, and a write back register for holding data received from the RAM and selectively providing that data to a system port." Thus, these arguments from the inventor apply to narrow the claims.

Similarly, the inventor had to amend the claims of the Chan '241 patent 4 times, each time incorporating additional structure and features to its computer system claims before the PTO granted the patent. To gain allowance, the inventor argued that the claims covered a computer system including, among other things, "a dual port cache memory coupled between a host processor and a system memory" with "one [port] connected to a host data bus of the system memory" and "having registers coupling cache storage locations to a host port and to a system port, wherein a data path between the host data bus and the system data bus is operably decoupled by buffering and selective provision of data to and from the cache storage locations by

the registers, so as to allow concurrent transfer of data to and from the dual port cache memory." Again, these inventor arguments apply to narrow the claims.

Given the limited nature of ProMOS's exclusion rights under its patents and the vast scope of permissible use of cache memory, ProMOS cannot rightfully claim all products using a cache memory, and cannot legitimately assert its patents against any product which does not have the specific structure and functionality which was required for patent issuance. Yet ProMOS has refused to limit its allegations of infringement to products meeting the above criteria and has failed to give any explanation as to how it could legitimately maintain a claim scope broad enough to cover products which do not meet these criteria.

THE FORTIN PATENT

As far as the Fortin patent, Fortin explicitly surrendered any claim to coverage of any processes that form a layer of titanium nitride by chemical vapor deposition ("CVD"). Nevertheless, ProMOS has persisted in accusing processes of Freescale that form a titanium nitride layer by CVD, without providing any explanation of how a CVD process could possibly infringe when ProMOS is estopped from asserting its patent against CVD processes. The Fortin patent claims "forming a titanium nitride layer over the structure by physical vapor deposition…" or some variation thereof in every claim. To overcome prior art cited by the Examiner during prosecution of the Fortin patent (the cited prior art is, in fact, a Motorola patent which discloses the steps claimed by Fortin), the inventor specifically distinguished between physical vapor deposition ("PVD") and CVD, and then represented to the PTO that "[i]n any event, CVD is not PVD or a type of PVD" (*see*, Amendment dated July 30, 2002, at p. 9).

During this litigation, however, ProMOS has tried to obfuscate the well-known and previously-admitted differences between PVD and CVD. ProMOS has made vague and

untenable suggestions, without regard to the most basic of legal requirements governing the construction of patent claims, that somehow the terminology surrounding PVD and CVD has become unclear over the past few years (*see*, *e.g.*, ProMOS's response to Freescale's Interrogatory No. 18: "[T]he line between chemical vapor deposition and physical vapor deposition [is not] well settled. Indeed more recent developments in the art have blurred that line."). Moreover, ProMOS has not even attempted to offer any evidence to support this litigation-induced assertion. Instead, ProMOS has deliberately avoided providing any contention regarding the meaning of the Fortin claim terms. In any case, the Fortin patent claims cannot be construed to cover any process, including as used by Freescale, that forms a layer of titanium nitride by chemical vapor deposition.

* *

Given the explicit claim language, the patent specifications, and the prosecution history, it is clear that the Patents-in-Suit cannot be given a construction that is broad enough to cover Freescale's products.

INTERROGATORY NO. 20:

Describe in detail each test or analysis of any Freescale product conducted by or on behalf of Freescale to determine whether such product infringes, including for each such test or analysis, the date(s) thereof, the name(s) and employer of the individual(s) who conducted such test or analysis, and the results of and conclusions drawn from such test or analysis, identify each person with knowledge of each such test or analysis, and identify all documents that relate to each such test or analysis.

RESPONSE:

In addition to its General Objections, Freescale objects to this interrogatory to the extent it seeks information, documents, or things protected under the attorney-client privilege or the attorney work product doctrine, and as premature in light of the date in the Rule 16 Scheduling Order for Freescale to decide whether to rely on advice of counsel and to produce

CERTIFICATE OF SERVICE

I hereby certify that on August 30, 2007, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF which will send electronic notification of such filing to the following:

John G. Day, Esquire
Steven J. Balick, Esquire
ASHBY & GEDDES

Additionally, I hereby certify that true and correct copies of the foregoing were caused to be served on August 30, 2007 upon the following individuals in the manner indicated:

BY E-MAIL AND HAND DELIVERY

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/s/ Mary B. Graham (#2256)

Mary B. Graham (#2256)